PDP-11

Phase 1

**Team Number** 3

**Team Members**

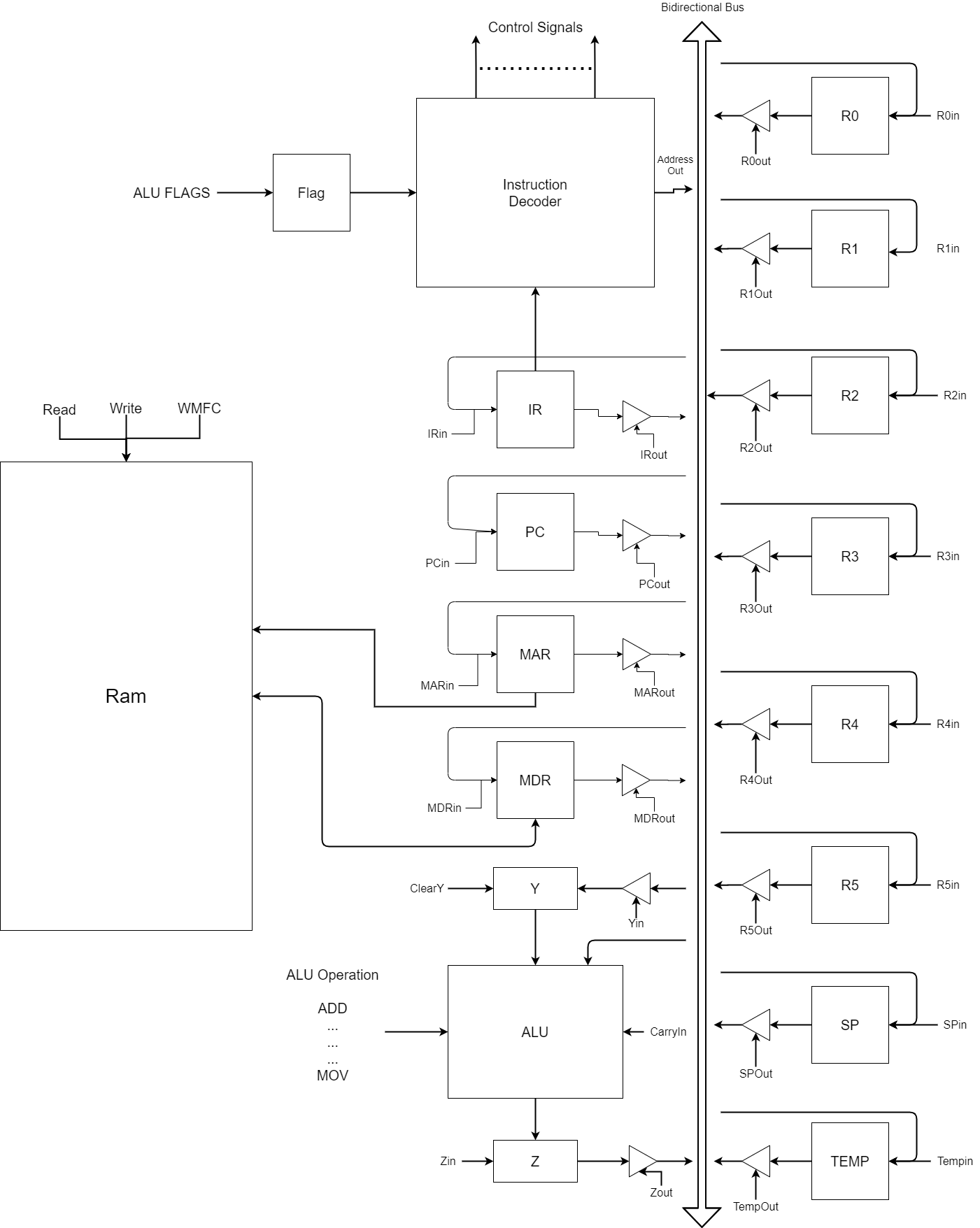
Ahmed Mostafa

Seif El Din El Said

Omar Ibrahim

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**Bus System Schematic:**

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**Instruction Set Architecture:**

* **2-Operands Instructions:**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Op code | | | | src | | | | | | dst | | | | | |
| **15** | **14** | **13** | **12** | **11** | **10** | **9** | **8** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |

|  |  |
| --- | --- |
| Instruction | Op code (Binary) |
| MOV | 0000 |
| ADD | 0001 |
| ADC | 0010 |
| SUB | 0011 |
| SBC | 0100 |
| AND | 0101 |
| OR | 0110 |
| XOR | 0111 |
| CMP | 1000 |

* **1-Operand Instructions:**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| OP code | | | | | | | | | | | dst | | | | |
| **15** | **14** | **13** | **12** | **11** | **10** | **9** | **8** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |

|  |  |
| --- | --- |
| Instruction | Op code (Binary) |
| INC | 1001 00 0000 |
| DEC | 1001 00 0100 |
| CLR | 1001 00 1000 |
| INV | 1001 00 1100 |
| LSR | 1001 01 0000 |
| ROR | 1001 01 0100 |
| ASR | 1001 01 1000 |
| LSL | 1001 01 1100 |
| ROL | 1001 10 0000 |

* **Branch Instructions:**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| OP code | | | | | | | | Offset | | | | | | | |
| **15** | **14** | **13** | **12** | **11** | **10** | **9** | **8** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |

|  |  |
| --- | --- |
| Instruction | Op code (Binary) |
| BR | 1010 0000 |
| BEQ | 1010 0001 |
| BNE | 1010 0010 |
| BLO | 1010 0011 |
| BLS | 1010 0100 |
| BHI | 1010 0101 |
| BHS | 1010 0110 |

* **No Operand Instructions:**

|  |  |  |  |
| --- | --- | --- | --- |
| OP code | | | |
| **15** | **14** | **13** | **12** |

|  |  |
| --- | --- |
| Instruction | Op code (Binary) |
| BR | 1011 |
| BEQ | 1011 |
| BNE | 1011 |

**Micro-Instructions:**

* **Words:**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| F1 4 BITS |  | F2 3 BITS |  | F3 2 BITS |  | F4 1 BIT |  | F5 4 BITS |  |
| "0000" | **No Transfer** | "000" | **No Transfer** | "00" | **No transfer** | "0" | **No transfer** | "0000" | **ADD** |
| "0001" | **PC out** | "001" | **Pc in** | "01" | **MAR in** | "1" | **Yin** | "0001" | **ADC** |
| "0010" | **MDR out** | "010" | **IR in** | "10" | **MDR in** |  |  | "0010" | **SUB** |
| "0011" | **Z out** | "011" | **Zin** |  |  |  |  | "0011" | **SBC** |
| "0100" | **RSrc out** | "100" | **RSrc in** |  |  |  |  | "0100" | **AND** |
| "0101" | **RDst out** | "101" | **RDst in** |  |  |  |  | "0101" | **OR** |
| "0110" | **Temp out** | "110" | **Temp in** |  |  |  |  | "0110" | **XOR** |
| "0111" | **Address out** | "111" | **Branch** |  |  |  |  | "0111" | **INV** |
| "1000" | **HLT** |  |  |  |  |  |  | "1000" | **LSR** |
| "1001" | **RESET** |  |  |  |  |  |  | "1001" | **ROR** |
|  |  |  |  |  |  |  |  | "1010" | **ASR** |
|  |  |  |  |  |  |  |  | "1011" | **LSL** |
|  |  |  |  |  |  |  |  | "1100" | **ROL** |
|  |  |  |  |  |  |  |  | "1101" | **INC** |
|  |  |  |  |  |  |  |  | "1110" | **DEC** |
|  |  |  |  |  |  |  |  | "1111" | **MOV** |

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| F6 2 BITS |  | F7 1 BIT |  | F8 1 BIT |  | F9 1 BIT |  | F10 1 BIT |  |
| "00" | **No action** | "0" | **No action** | "0" | **Carry-in=0** | "0" | **No actions** | "0" | **Continue** |
| "01" | **Read** | "1" | **Clear Y** | "1" | **Carry-in=1** | "1" | **WMFC** | "1" | **END** |
| "10" | **Write** |  |  |  |  |  |  |  |  |
| "11" | **uBranch** |  |  |  |  |  |  |  |  |